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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/854,865	05/14/2001	Michael Philip McIntosh	TUC920010006US1	9915

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INTERNATIONAL BUSINESS MACHINES CORPORATION
9000 SOUTH RITA ROAD
TUCSON, AZ 85744

EXAMINER	
KNOLL, CLIFFORD H	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 10/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/854,865	MCINTOSH ET AL.	
	Examiner	Art Unit	
	Clifford H Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to communication filed 7/14/2004. Currently claims 1-36 are pending.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

Claims 1-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Beyers (US 6072804).

Regarding claim 1, Beyers discloses a plurality of individual frames connected in series, a multi-channel bus coupled to each frame (e.g., col. 2, line 66 – col. 3, line 12), a power bus return bus carrying information indicative of the last frame (e.g., col. 3, lines 10-12), where one of the frames is a first frame (e.g., col. 4, lines 17-20) a signal indicative of power being supplied to it and generating a delayed signal each subsequent frame receiving said delayed signal and generating a further delayed signal and each frame generating a pulse on said frame bus (e.g., col. 4, lines 15-17), one of said frames being defined as said last frame and receiving said delayed signal and generating a signal to activate said power return bus (e.g., col. 4, lines 26-31) and

wherein the total count counter being incremented by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 2, Beyers also discloses where the total count counter represents the total number connected together (e.g., col. 19, lines 22-24).

Regarding claim 3, Beyers also discloses wherein at least one said frame generates a frame pulse (e.g., col. 4, lines 15-17).

Regarding claim 4, Beyers also discloses an ID counter being incremented by each said pulse (e.g., col. 8, line 6).

Regarding claim 5, Beyers also discloses the ID counter represents the individual ID (e.g., col. 8, line 6).

Regarding claim 6, Beyers also discloses the delayed signal has an approximately constant predetermined value (e.g., col. 6, lines 28-30).

Regarding claim 7, the delayed signal has a variable delay value (e.g., col. 6, lines 60-61).

Regarding claim 8, Beyers discloses a plurality of individual frames connected in series, a multi-channel bus coupled to each frame (e.g., col. 2, line 66 – col. 3, line 12), a power bus return bus carrying information indicative of the last frame (e.g., col. 3, lines 10-12), where one of the frames is a first frame (e.g., col. 4, lines 17-20) a signal indicative of power being supplied to it and generating a delayed signal each subsequent frame receiving said delayed signal and generating a further delayed signal and each frame generating a pulse on said frame bus (e.g., col. 4, lines 15-17), one of said frames being defined as said last frame and receiving said delayed signal and

generating a signal to activate said power return bus (e.g., col. 4, lines 26-31) and wherein the total count counter being incremented by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 9, Beyers also discloses where the total count counter represents the total number connected together (e.g., col. 19, lines 22-24).

Regarding claim 10, Beyers also discloses wherein at least one said frame generates a frame pulse (e.g., col. 4, lines 15-17).

Regarding claim 11, Beyers also discloses an ID counter being incremented by each said pulse (e.g., col. 8, line 6).

Regarding claim 12, Beyers also discloses the ID counter represents the individual ID (e.g., col. 8, line 6).

Regarding claim 13, Beyers discloses coupling a plurality of individual frames connected in series, a multi-channel bus coupled to each frame (e.g., col. 2, line 66 – col. 3, line 12), designating a last frame (e.g., col. 3, lines 10-12), designating one of the frames as a first frame (e.g., col. 4, lines 17-20) receiving a signal indicative of power being supplied to it and generating a delayed signal each subsequent frame receiving said delayed signal and generating a further delayed signal and each frame generating a pulse on said frame bus (e.g., col. 4, lines 15-17), generating a signal to activate said power return bus (e.g., col. 4, lines 26-31) and incrementing a register by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 14, Beyers also discloses generating a frame pulse and incrementing a register (e.g., col. 19, lines 22-24).

Regarding claim 15, Beyers also discloses the ID counter represents the individual ID (e.g., col. 8, line 6).

Regarding claim 16, Beyers also discloses where the total count counter represents the total number connected together (e.g., col. 19, lines 22-24).

Regarding claim 17, Beyers discloses a plurality of individual frames connected in series, a multi-channel bus coupled to each frame (e.g., col. 2, line 66 – col. 3, line 12), a power bus return bus carrying information indicative of the last frame (e.g., col. 3, lines 10-12), where one of the frames is a first frame (e.g., col. 4, lines 17-20) a signal indicative of power being supplied to it and generating a delayed signal each subsequent frame receiving said delayed signal and generating a further delayed signal and each frame generating a pulse on said frame bus (e.g., col. 4, lines 15-17), one of said frames being defined as said last frame and receiving said delayed signal and generating a signal to activate said power return bus (e.g., col. 4, lines 26-31) and wherein the individual ID counter being incremented by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 18, Beyers also discloses where the total count counter represents the total number connected together (e.g., col. 19, lines 22-24).

Regarding claim 19, Beyers also discloses a power return bus carrying information indicative of the last frame and receiving said delayed signal and generating a signal to activate said power return bus (e.g., col. 4, lines 26-31).

Regarding claim 20, Beyers also discloses the total count counter being incremented by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 21, Beyers also discloses where the total count counter represents the total number connected together (e.g., col. 19, lines 22-24).

Regarding claim 22, Beyers discloses a plurality of individual frames connected in series, a multi-channel bus coupled to each frame (e.g., col. 2, line 66 – col. 3, line 12), a power bus return bus carrying information indicative of the last frame (e.g., col. 3, lines 10-12), where one of the frames is a first frame (e.g., col. 4, lines 17-20) a signal indicative of power being supplied to it and generating a delayed signal each subsequent frame receiving said delayed signal and generating a further delayed signal and each frame generating a pulse on said frame bus (e.g., col. 4, lines 15-17), one of said frames being defined as said last frame and receiving said delayed signal and generating a signal to activate said power return bus (e.g., col. 4, lines 26-31) and wherein the individual ID counter being incremented by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 23, Beyers also discloses the ID counter represents the individual ID (e.g., col. 8, line 6).

Regarding claim 24, Beyers also discloses a power return bus carrying information indicative of the last frame and receiving said delayed signal and generating a signal to activate said power return bus (e.g., col. 4, lines 26-31).

Regarding claim 25, Beyers also discloses the total count counter being incremented by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 26, Beyers also discloses where the total count counter represents the total number connected together (e.g., col. 19, lines 22-24).

Regarding claim 27, Beyers discloses coupling a plurality of individual frames connected in series, a multi-channel bus coupled to each frame (e.g., col. 2, line 66 – col. 3, line 12), designating a last frame (e.g., col. 3, lines 10-12), designating one of the frames as a first frame (e.g., col. 4, lines 17-20) receiving a signal indicative of power being supplied to it and generating a delayed signal each subsequent frame receiving said delayed signal and generating a further delayed signal and each frame generating a pulse on said frame bus (e.g., col. 4, lines 15-17), generating a signal to activate said power return bus (e.g., col. 4, lines 26-31) and incrementing a register by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 28, Beyers also discloses generating a frame pulse and incrementing a register (e.g., col. 19, lines 22-24).

Regarding claim 29, Beyers also discloses the ID counter represents the individual ID (e.g., col. 8, line 6).

Regarding claim 30, Beyers also discloses where the total count counter represents the total number connected together (e.g., col. 19, lines 22-24).

Regarding claim 31, Beyers discloses a plurality of individual frames connected in series, a multi-channel bus coupled to each frame (e.g., col. 2, line 66 – col. 3, line

12), a power bus return bus carrying information indicative of the last frame (e.g., col. 3, lines 10-12), where one of the frames is a first frame (e.g., col. 4, lines 17-20) a signal indicative of power being supplied to it and generating a delayed signal each subsequent frame receiving said delayed signal and generating a further delayed signal and each frame generating a pulse on said frame bus (e.g., col. 4, lines 15-17), one of said frames being defined as said last frame and receiving said delayed signal and generating a signal to activate said power return bus (e.g., col. 4, lines 26-31) and wherein the total count counter being incremented by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 32, Beyers also discloses the ID counter represents the individual ID (e.g., col. 8, line 6).

Regarding claim 33, Beyers also discloses where the total count counter represents the total number connected together (e.g., col. 19, lines 22-24).

Regarding claim 34, Beyers discloses coupling a plurality of individual frames connected in series, a multi-channel bus coupled to each frame (e.g., col. 2, line 66 – col. 3, line 12), designating a last frame (e.g., col. 3, lines 10-12), designating one of the frames as a first frame (e.g., col. 4, lines 17-20) receiving a signal indicative of power being supplied to it and generating a delayed signal each subsequent frame receiving said delayed signal and generating a further delayed signal and each frame generating a pulse on said frame bus (e.g., col. 4, lines 15-17), generating a signal to activate said power return bus (e.g., col. 4, lines 26-31) and incrementing a register by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 35, Beyers also discloses the ID counter represents the individual ID (e.g., col. 8, line 6).

Regarding claim 36, Beyers also discloses where the total count counter represents the total number connected together (e.g., col. 19, lines 22-24).

Response to Arguments

Applicant's arguments filed 7/14/2004 have been fully considered but they are not persuasive.

Regarding claim 1, Applicant argues that Beyers does not disclose a "library frame in a multi-frame tape library system" (p. 13); however no library frame is recited, instead "individual frames" are recited as connected in series. At the passage cited supra, Beyers discloses "a daisy chained ring with an input and an output in each device or instrument" (col. 2, lines 65-66), which devices are interpreted as the frames of the claimed invention.

Applicant further argues that recitation of "'each said frame comprising a pulse signal generator and a delay signal generator, at least one said frame also comprising a total count counter' is nowhere disclosed in Beyers" (p. 13); however Beyers discloses precisely this: that each frame receives and generates a delayed signal ("each node goes through the same states as the previous node, delayed by one received word time plus cable propagation delay", col. 6, lines 28-30), and the total count counter is incremented ("[e]ach node that receives the name command, increments the number

represented by the node address bits, uses this number as its node address, and sends the name command with its own node address in the node address bits to the next node. The master stops circulation of the command when it receives it after it has circulated around the loop", col. 8, lines 5-11). Examiner determines that Beyers generates pulses, and counts by each pulse. Beyers' "master" device is interpreted as the frame, which comprises the "total count counter" inasmuch as it receives a total count from the pulses it receives on the multi-frame bus.

Applicant further argues in distinction to the claimed "multi-channel bus coupled to each said frame" that Beyers "discloses cables and connectors for a daisy chained ring, not a multi-channel bus" (p. 13); however, as established supra, Beyers' daisy chain bus constitutes the claimed multi-channel bus, and the "cables and connectors" constitute the coupling as claimed.

Applicant further argues that "[a] frame bus or power return bus are not disclosed in Beyers" (p. 13); however, as cited supra, Beyers discloses that the last frame senses it is the last frame and consequently "conditions the second switch 60 to couple the output register 50 to the wires of the reverse path at the input connector" (col. 4, lines 31-33). The reverse path is interpreted as the recited power return bus. The frame bus has already been discussed supra. The claim supports no distinction.

Applicant further argues that Beyers discloses a "first node of a daisy chain" and distinguishes the claimed "wherein one of said frames being defined as a first frame" by arguing that "a node is not a library frame"; however the distinction between Beyers' "node" and the claimed "frame" does not receive support in the recitation.

Applicant further argues that Beyers does not disclose being "adapted to receive a signal indicative of power being supplied to any one of said frames and generat[ing] a delayed signal, each subsequent frame receiving said delayed signal and generating a further delayed signal, and each frame generating a pulse on said frame bus" (p. 14); however, as discussed supra this is precisely the interpretation of Beyers and the explanation is duplicated here: each frame receives and generates a delayed signal ("each node goes through the same states as the previous node, delayed by one received word time plus cable propagation delay", col. 6, lines 28-30). This is the result of the delayed signal generated by each device in the daisy-chain coupled system of Beyers.

Applicant further argues that Beyers does not disclose "wherein one of said frames being defined as said last frame and receiving said delayed signal and generating a signal to activate said power return bus" (p. 14); however, this has been treated supra, and duplicated here: Beyers discloses that the last frame senses it is the last frame and consequently "conditions the second switch 60 to couple the output register 50 to the wires of the reverse path at the input connector" (col. 4, lines 31-33). The reverse path is interpreted as the power return bus as recited.

Applicant further argues that Beyers does not disclose a total count counter being incremented by each said pulse" (pp. 14-15); however this has been established supra and is duplicated here: The master stops circulation of the command when it receives it after it has circulated around the loop", col. 8, lines 5-11). Beyers is determined to generate pulses, and is determined to count by each pulse. In this

interpretation Beyers' "master" device is the frame comprises the "total count counter" inasmuch as it receives a total count from the pulses it receives on the multi-frame bus.

Regarding claim 8, Applicant argues for distinction of the claimed plurality of individual frames connected in series, at least one frame also comprising a total count counter" (p. 15), the "multi-channel bus for exchanging information" (p.15), "a power bus return bus carrying information indicative of the last frame" (p. 16), and "where one of said frames is a first frame" (p.16). These distinctions have been raised regarding claim 1, and have been adequately dealt with in this regard supra.

Regarding claims 13 and 34, Applicant argues for distinction of the claimed "method to automatically detect the total count of frames within a modular multi-frame tape library system" (pp. 16-17); however, as discussed supra, Beyers discloses the total count counter is incremented ("[e]ach node that receives the name command, increments the number represented by the node address bits, uses this number as its node address, and sends the name command with its own node address in the node address bits to the next node. The master stops circulation of the command when it receives it after it has circulated around the loop", col. 8, lines 5-11). Beyers is determined to generate pulses, and is determined to count by each pulse. Beyers' "master" device is the frame, which comprises the "total count counter" inasmuch as it receives a total count from the pulses it receives on the multi-frame bus.

Applicant further argues for distinction of "coupling a plurality of frames to a multi-channel data bus comprising a frame bus and a power return bus; however, as dealt

with regarding claim 1, Beyers discloses a daisy-chain bus, interpreted as the claimed frame bus, as well as the reverse bus, interpreted as the power return bus.

Applicant notes that "Beyers only mentions 'power' in one instance regarding power up of the system" (p. 17); however, this is not relied upon in the interpretation of Beyer. Any particular distinction from Beyer's "reverse bus" to "power bus" in the claims lacks support for that distinction.

Applicant further argues for distinction for "designating one of said frames as a last frame", or "first frame" (p. 17); "said first frame receiving a signal indicative of power being supplied to any one of said frames and generating a first delayed signal and a pulse indicative of the presence of said first frame" (p. 17); "generating a signal to activate said power return bus when said delayed signal reaches said last frame" (p. 18), and "incrementing a register by each pulse until said power bus is activated"; however each of these issues has been raised regarding claim 1, and has been treated adequately regarding claim 1 supra.

Regarding claim 17, Applicant argues for distinction of "a plurality of individual frames connected in series, each said frame comprising a pulse signal generator and a delay signal generator, at least one said frame also comprising an individual ID counter" (p. 19), "a multi-channel bus coupled to each frame" (p. 19), "a frame bus for carrying information indicative of the presence of each said frame", "one of said frames being defined as a first frame" (p. 19), "a signal indicative of power being supplied to any one of said frames and generate a delayed signal ...." p. 20),

Regarding claim 22, Applicant argues for distinction of "a plurality of individual frames connected together in series" (p. 21), "a multi-channel bus" (p. 22), "one of said frames being defined as a first frame" (p. 22), receipt of "a signal indicative of power being supplied to any one of said frames and generat[ing] a pulse..." (p. 22), and the "counter being incremented by each said pulse" (p. 23); however these arguments have been dealt with adequately regarding preceding claims supra.

Regarding claim 27, Applicant argues for distinction of detecting "the total count of frames" (p. 23), "coupling a plurality of frames" (p. 24), "designating one of said frames as a last frame" (p. 24), "designating one of said frames as a first frame" (p. 24), "receiving a signal indicative of power being supplied" (p. 24), "supplying said delayed signal..." (p. 25).

Thus the rejection of claims 1-36 is maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 571-272-3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

chk

Khanh Dang
Primary Examiner